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1 **Scheduling designs into a time-multiplexed FPGA**   ■
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   An algorithm is presented for partitioning a design in time. The algorithm devides a large,
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   includes facilities for optimizing the partitioning to improve routability, for fitting the
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2 **Buffer minimization and time-multiplexed I/O on dynamically reconfigurable FPGAs**   ■
   Douglas Chang, Malgorzata Marek-Sadowska
   February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-
                programmable gate arrays**
   Publisher: ACM Press
   Full text available: 📄 pdf(1.10 MB)   Additional Information: full citation, references, citings, index terms

3 **Network flow based circuit partitioning for time-multiplexed FPGAs**   ■
   Huiqun Liu, D. F. Wong
   November 1998 **Proceedings of the 1998 IEEE/ACM international conference on
                Computer-aided design**
   Publisher: ACM Press
   Full text available: 📄 pdf(957.50 KB)   Additional Information: full citation, references, citings, index terms

4 **A graph theoretic optimal algorithm for schedule compression in time-multiplexed**   ■
   FPGA partitioning
   Huiqun Liu, D. F. Wong
   November 1999 **Proceedings of the 1999 IEEE/ACM international conference on
                Computer-aided design**